

# **JEDEC STANDARD**

---

## **Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing**

---

### **JESD22-A113F**

(Revision of JESD22A113E, March 2006)

OCTOBER 2008

---

**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



## NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or [www.jedec.org](http://www.jedec.org)

Published by  
©JEDEC Solid State Technology Association 2008  
3103 North 10th Street  
Suite 240 South  
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

**PRICE: Please refer to the current  
Catalog of JEDEC Engineering Standards and Publications online at  
<http://www.jedec.org/Catalog/catalog.cfm>**

Printed in the U.S.A.  
All rights reserved

PLEASE!

DON'T VIOLATE  
THE  
LAW!

This document is copyrighted by JEDEC and may not be reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association  
3103 North 10th Street  
Suite 240 South  
Arlington, VA 22201-2107  
or call (703) 907-7559



## **TEST METHOD A113F**

# **PRECONDITIONING OF NONHERMETIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING**

---

### **Foreword**

---

This document provides an industry standard test method for preconditioning components that is representative of a typical industry multiple solder reflow operation.

---

### **Introduction**

---

The typical use of surface mount devices (SMD) involves subjecting the SMDs to elevated temperatures during board assembly, which combined with moisture in the package can induce internal package damage that could be a reliability concern. Preconditioning of SMD packages is used to simulate the effects of board assembly on moisturized packages, prior to reliability testing. This allows reliability testing at the component level on as shippable products with a board assembly simulation. During preconditioning, test samples are subjected to temperature cycling (optional), dry bake, moisture soaking, solder reflow simulation, flux, rinse, dry, and electrical test before reliability testing.



**TEST METHOD A113F****PRECONDITIONING OF NONHERMETIC SURFACE MOUNT DEVICES  
PRIOR TO RELIABILITY TESTING**

(From JEDEC Board ballot JCB-08-46, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

---

**1 Scope**

---

This Test Method establishes an industry standard preconditioning flow for nonhermetic solid state SMDs that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in-house reliability testing (qualification and reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow).

**NOTE:** Correlation of moisture-induced stress sensitivity (per J-STD-020 and JESD22-A113) and actual reflow conditions used are dependent upon identical temperature measurement by both the semiconductor manufacturer and the board assembler. Therefore, it is recommended that the package temperature at the top center of package be determined during assembly board reflow profile setup, to ensure that it does not exceed the temperature at which the components are evaluated, based on package thickness and volume as stated in IPC/JEDEC J-STD-020.

---

**2 Normative reference**

---

IPC/JEDEC J-STD-020 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

JESD22-A104 Temperature Cycling

JESD625 Requirements for Handling Electrostatic Discharge Sensitive (ESD) Devices

JESD47 Stress-Test-Driven Qualification of Integrated Circuits

JESD94 Application Specific Qualification Using Knowledge Based Test Methodology

---

### **3 Apparatus**

---

This test method requires use of the following equipment.

#### **3.1 Moisture chamber temperature**

Moisture chamber(s) capable of operating at 85 °C/85% RH, 85 °C/60% RH, and 30 °C/60% RH. Within the chamber working area, temperature tolerance must be  $\pm 2$  °C and the RH tolerance must be  $\pm 3\%$  RH. A chamber with 60 °C/60% RH capability is optional for accelerated soak conditions (See J-STD-020).

#### **3.2 Solder reflow equipment**

- a) (Preferred) - Full Convection reflow system capable of maintaining the reflow profiles required by this standard.
- b) Infrared (IR)/Convection solder reflow equipment capable of maintaining the reflow profiles required by this standard. It is required that this equipment use IR to heat only the air and not directly impinge upon the SMD Packages/devices under test.

NOTE The moisture sensitivity classification test results are dependent upon the package body temperature (rather than the reflow carrier and or package terminal temperature).

#### **3.3 Optical microscope**

Optical Microscope (40x for external visual exam).

#### **3.4 Electrical test equipment**

Electrical test equipment capable of performing room temperature dc and functional tests.

#### **3.5 Bake oven**

Bake oven capable of operating at 125  $\pm 5/0$  °C.

#### **3.6 Temperature Cycle Chamber**

Temperature Cycle Chamber capable of operating, as a minimum, over the range of (-40  $\pm 0/-10$ ) °C to (60 °C  $\pm 10/0$ ) °C per JESD22-A104. This equipment is only required if optional Step 4.3 is used.

---

## **4 Test procedure**

---

Using similar components, it is recommended that the moisture sensitivity level (MSL), per J-STD-020, be determined before starting the preconditioning sequence to establish which moisture soak condition is appropriate, i.e., likely to pass. If the MSL level is not known then other relevant moisture evaluation data may be consulted, or an arbitrary selection may be made. Multiple moisture soak conditions can also be run to determine a passing level. However, the soak condition used must be consistent with the floor life information in IPC/JEDEC J-STD-020.

Reflow requirements are provided for both SnPb and Pb-free conditions and should be used based on the intended end use of the component. The same package may have different MSL levels depending on whether the SnPb or Pb-free reflow is used.

At all times the test parts should be handled using proper ESD procedures in accordance with JESD625.

Refer to Annex A for the typical test flow.

**NOTE** If the preconditioning sequence is being performed by the semiconductor manufacturer, steps 4.1, 4.2, and 4.4 are optional since they are the supplier's risks. If the preconditioning sequence is being performed by the user, steps 4.7 through 4.9 are optional.

### **4.1 Initial electrical test**

Perform electrical and/or functional test to verify that the devices meet the room temperature data sheet specification. Replace any devices that fail to meet this requirement.

### **4.2 Visual inspection**

Perform an external visual examination under 40X optical magnification to ensure that no devices with external cracks or other damage are used in this test method. If mechanical rejects are found, corrective action must be implemented in the manufacturing process and a new sample must be drawn from product that has been processed with the corrective action.

### **4.3 Temperature cycling**

Perform five (5) cycles of temperature cycle from -40 °C (or lower) to 60 °C (or higher) to simulate shipping conditions. Acceptable alternative test conditions and temperature tolerances are A through I and L through N as defined in Table 1 of JESD22-A104, Temperature Cycling. This step is optional based on product requirements.

## **4 Test procedure (cont'd)**

### **4.4 Bake out**

Bake the devices for 24 hours minimum at  $125 \pm 5/-0$  °C. This step is intended to remove all moisture from the package so that it will be “dry.”

NOTE This time/temperature may be modified if desorption data on the particular device being preconditioned shows that a different condition is required to obtain a "dry" package. Refer to J-STD-020 for procedures on running absorption and desorption curves.

### **4.5 Moisture Soak**

Place devices in a clean, dry, shallow container so that the package bodies do not touch or overlap each other. Submit each sample to the appropriate moisture soak requirements shown in IPC/JEDEC J-STD-020. The moisture soak should be initiated within 2 hours of bake.

NOTE The moisture soak is optional for devices (Flip Chip die, etc.) where moisture absorption data is available showing the particular device being preconditioned does not absorb moisture. Refer to J-STD-020 for procedures on running absorption and desorption curves.

### **4.6 Reflow**

Not sooner than 15 minutes and not longer than 4 hours after removal from the temperature/humidity chamber, subject the sample to 3 cycles, Note 1, of the appropriate reflow conditions. The reflow conditions are defined in IPC/JEDEC J-STD-020. If the timing between removal from the temperature/humidity chamber and initial reflow cannot be met then the parts must be rebaked and resoaked according to 4.4 and 4.5.

NOTE 1 The 3 cycles for the component represent the following:

- Cycle 1 - the first pass of a Double-Sided, Double-Pass (DSDP) assembly reflow process.
- Cycle 2 - the second pass of a DSDP assembly reflow process.
- Cycle 3 - rework of a near neighbor component on the assembly where the component being classified experiences reflow-like temperatures.

NOTE 2 If the reflow cycle regimen is not representative for the component being classified, refer to JESD94 for application specific qualification guidance.

The sample parts shall be cooled sufficiently (preferably back to room temperature) between reflow cycles so that the reflow temperatures/times of the samples are not affected on the subsequent reflow cycles.

Reflow practices shall be sufficient to ensure that all sample parts, in each reflow cycle, will meet the appropriate reflow profile requirements of IPC/JEDEC J-STD-020.

Components intended for use in a “Pb-free” assembly process shall be evaluated using the “Pb-free” reflow temperature whether or not the component is Pb-free.

## **4 Test procedure (cont'd)**

### **4.6 Reflow (cont'd)**

If parts are reflowed in other than the normal assembly reflow orientation (i.e. live bug/dead bug) the damage response should be correlated.

The reflow oven should be loaded with the same configuration when running preconditioning as was used to develop the reflow profile.

The reflow profiles in IPC/JEDEC J-STD-020 are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in IPC/JEDEC J-STD-020.

#### **4.6.1 Solder attachment after reflow**

If reliability testing is to be performed in a second level configuration, one of the reflow cycles may be used to attach the device to the test board. If the board assembly is to be performed at a later time than the devices, at the user discretion, can be baked and vacuum sealed until such time that it is solder attached to the test board or facsimile. Since the board attachment replicates a real life process with flux application, reflow and cleaning, steps 4.7 and 4.8 are no longer necessary or mandated prior to submission to reliability stress testing. Flux type shall be documented per section 6.

#### **4.7 Flux application**

After the reflow solder cycles are completed, allow the devices to cool at room ambient for 15 minutes minimum. Devices shall then be dipped (full body immersion) in an activated water soluble flux at room ambient for 10 seconds minimum.

Ball Grid Array (BGA), Column Grid Array (CGA) and organic substrate Land Grid Array (LGA) packages do not require flux dipping because their typical board application methods do not use liquid fluxes. Steps 4.8 and 4.9 are not required when flux dipping is omitted for these package types.

#### **4.8 Cleaning**

Clean devices externally using multiple agitated deionized water rinses. No waiting time is required between flux application and cleaning. Ensure all flux residuals are completely removed.

#### **4.9 Drying**

Devices should be dried at room ambient prior to submission to reliability testing.

## **4 Test procedure (cont'd)**

### **4.10 Final electrical test**

Submit the devices to electrical and/or functional testing per the room temperature data sheet specification. For the semiconductor manufacturer, this step is optional and may be omitted since it is a supplier's risk. Any valid failures found at this point due to the preconditioning sequence indicate that the device may have been classified in the wrong level or something is substandard with the test devices. Failure analysis should be conducted. If appropriate, this device type should be reevaluated to determine the correct moisture sensitivity level. This would require resubmitting a sample to the correct level preconditioning sequence prior to reliability testing per 5.

---

## **5 Applicable reliability tests**

---

SMDs should be subjected to the appropriate preconditioning sequence of this document prior to being submitted to reliability tests per JESD47 or the semiconductor manufacturer's in-house reliability procedures.

---

## **6 Summary**

---

The following details shall be specified in the applicable procurement document.

- a) Rev of IPC/JEDEC J-STD-020 used for the reflow profile.
- b) Number of reflow cycles if other than three.
- c) Type of flux if other than Step 4.7.
- d) Reliability tests if other than 5.
- e) Test conditions and duration of reliability tests in 5.
- f) Electrical test description, including test temperature(s).

---

**Annex A Typical Preconditioning Sequence Flow**


---

Step	Item	Details	Section
1	Initial Electrical Test	<ul style="list-style-type: none"> <li>- Replace any failing devices</li> <li>- Optional for testing by Supplier</li> </ul>	4.1
2	Visual Inspection	<ul style="list-style-type: none"> <li>- Replace any failing devices</li> <li>- Optional for testing by Supplier</li> </ul>	4.2
3	Temperature Cycling	<ul style="list-style-type: none"> <li>- 5 cycles -40 °C to 60 °C</li> <li>- Optional shipping simulation based on product requirements</li> </ul>	4.3
4	Bake	<ul style="list-style-type: none"> <li>- 24 h at 125 °C</li> <li>- Optional for testing by Supplier</li> </ul>	4.4
5	Moisture Soak	<ul style="list-style-type: none"> <li>- Soak time and conditions per IPC/JEDEC J-STD-020 based on device MSL level</li> </ul>	4.5
6	Reflow	<ul style="list-style-type: none"> <li>- 3 reflow cycles using profiles per IPC/JEDEC J-STD-020, document rev of J-STD-020 used</li> <li>- SnPb or Pb-free profile based on device end use process</li> </ul>	4.6
7	Flux Application	<ul style="list-style-type: none"> <li>- 10 s full immersion dip in activated water soluble flux</li> <li>- Optional for testing by User or second level configuration</li> <li>- Not required for BGA, CGA and LGA packages</li> </ul>	4.7
8	Cleaning	<ul style="list-style-type: none"> <li>- DI water rinse</li> <li>- Remove all flux residual</li> <li>- Optional for testing by User or second level configuration</li> <li>- Not required for BGA, CGA and LGA packages</li> </ul>	4.8
9	Drying	<ul style="list-style-type: none"> <li>- Room ambient drying</li> <li>- Optional for testing by User or second level configuration</li> <li>- Not required for BGA, CGA and LGA packages</li> </ul>	4.9
10	Final Electrical Test	<ul style="list-style-type: none"> <li>- <b>If all devices pass then ready for Reliability Testing</b></li> <li>- If valid failures are found then devices may have been tested to the wrong MSL level or something is substandard with the devices</li> <li>- Optional for testing by Supplier</li> </ul>	4.10

---

**Annex B (informative) Differences between JESD22-A113F and JESD22-A113E**

---

The following list briefly describes most of the changes made to entries that appear in this standard, JESD22-A113F, compared to its predecessor, JESD22-A113E (March 2006). If the change to a concept involves any words added or deleted, it is included. Punctuation changes may not be included.

<b>Page</b>	<b>Description of change</b>
2	Added reference to JESD47 and JESD94
4	4.5 added Note, Flip Chip moisture soak exception
4	4.6 added Note 1, Description of reflow cycles
4	4.6 added Note 2, Reference to JES94 for guidance



---

**Standard Improvement Form****JEDEC JESD22-A113F**

---

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC  
Attn: Publications Department  
3103 North 10th Street  
Suite 240 South  
Arlington, VA 22201-2107  
Fax: 703.907.7583

---

1. I recommend changes to the following:

Requirement, clause number \_\_\_\_\_

Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

Unclear  Too Rigid  In Error

Other \_\_\_\_\_

---

2. Recommendations for correction:

---

---

---

---

---

3. Other suggestions for document improvement:

---

---

---

---

---

Submitted by

Name: \_\_\_\_\_

Phone: \_\_\_\_\_

Company: \_\_\_\_\_

E-mail: \_\_\_\_\_

Address: \_\_\_\_\_

City/State/Zip: \_\_\_\_\_

Date: \_\_\_\_\_

---

***JEDEC***

The JEDEC logo is centered on the page. It features the word "JEDEC" in a bold, italicized, dark green sans-serif font. Below the text is a red horizontal line that tapers to a point on the right side.