

Annex A (informative) Differences between JESD21C, Release 18/18A, and JESD21C, Release 17.

This table briefly describes most of the changes made to this standard, JESD21C, Release 18/18A, compared to its predecessor, JESD21C, Release 17. Some editorial changes are not included.

Section/ Page	Description of Change
3.6.3	Per JCB-07-016 and JCB-07-044 Added Section, LPDDR NVRAM
3.11.5.5	Per JCB-08-016 Updated section with DDR2(X32) EMR specifics.
3.12.1	Per JCB-08-014 Added Figure 9 – Ball Configuration for eMMC+LPDDR+A/D Muxed NOR/NAND MCP Per JCB-08-085 Rescinded Figures 1, 4, 5, 6, and 7. Added Figure 10 – 186-ball, Flash + DRAM (X16), Dual-bus 0.65 pitch Figure 11 – Flash + LPDDR/PSRAM x48 Multi-Bus Ballout Solution
3.12.2	Per JCB-08-036 and JCB-08-037 Added Figure 21 – PoP 14X14 mm body size, 0.65 mm pad pitch based on a true split DRAM and Non-volatile bus structure Added Figure 22 – PoP 12X12 mm body size, 0.50 mm pad pitch based on a true split DRAM and Non-volatile bus structure
4.1	Editorial Updated Section 4.1 TOC
4.1.2	Per JCB-08-012 Updated Section, SPD General Standard
4.1.2.11	Per JCB-08-049 Added Annex K: Serial Presence Detect (SPD) for DDR3 SDRAM, to Revision 1.0
4.1.4	Per JCB-08-0487 Added Section, Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor
4.20	Updated Table of Contents
4.20.10	Per JCB-08-055 Updated Section, PC2-6400/PC2-5300/PC2-4200/PC2-3200 Registered DIMM, to Revision 3.98
4.20.11	Per JCB-08-003 Updated Section, PC2-6400/PC2-5300/PC2-4200/PC2-3200 DDR2 SDRAM Unbuffered SO-DIMM Reference Design Specification, Rev. 2.5
4.20.13	Per JCB-08-017 Updated Section, PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Unbuffered DIMM Design Specification, Revision 3.1
4.20.18	Per JCB-08-076 Updated Section, PC3/6400/OC3-8500/PC3-10600/PC3-12800 DDR3 Unbuffered SO-DIMM Design Specification, Revision 1.0

Annex A (informative) Differences between JESD21C, Release 18/18A, and JESD21C, Release 17.

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Section/ Page	Description of Change
4.20.19	Per JCB-08-018 and JCB-08-66 Added Section, PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Unbuffered DIMM Design Specification, Revision 1.0
4.20.20	Per JCB-08-087 Added Section, PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification, Revision 0.84
4.20.20.A	Per JCB-08-025 Added Section, Annex A, R/C A, in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
4.20.20.B	Per JCB-08-020 Added Section, Annex B, R/C B, in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
4.20.20.C	Per JCB-08-021 Added Section, Annex C, R/C C, in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
4.20.20.D	Per JCB-08-056 Added Section, Annex D, R/C D, in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
4.20.20.E	Per JCB-08-083 Added Section, Annex E, R/C E, in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
4.20.20.F	Per JCB-08-057 Added Section, Annex F, R/C F, in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
4.20.20.G	Per JCB-08-052 Added Section, Annex G, R/C G, in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
4.20.20.H	Per JCB-08-053 Added Section, Annex H, R/C H, in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
4.20.20.J	Per JCB-08-019 Added Section, Annex J, R/C J, in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
4.20.20.K	Per JCB-08-054 Added Section, Annex K, R/C K in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
4.20.20.L	Per JCB-08-050 Added Section, Annex L, R/C L in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification

Annex A (informative) Differences between JESD21C, Release 18/18A, and JESD21C, Release 17.

This table briefly describes most of the changes made to this standard, JESD21C, Release 18/18A, compared to its predecessor, JESD21C, Release 17. Some editorial changes are not included.

Section/ Page	Description of Change
4.20.20.M	Per JCB-08-051 Added Section, Annex M, R/C M in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification
A-1	Updated Annex A (Informative) Differences between Release 18 and Release 17 of JESD21C.

Annex A.1 (informative) Differences between JESD21C, Release 17, and JESD21C, Release 16.

This table briefly describes most of the changes made to this standard, JESD21C, Release 17, compared to its predecessor, JESD21C, Release 16. Some editorial changes are not included.

Section/ Page	Description of Change
3.7.10	Per JCB-07-104 Added Section, High Speed DDR SRAM in 165 BGA
3.11.4	Per JCB-07-108 Added Figure 37 – 256M - 2G x32 DDR2 SDRAM in 128-Ball BGA
3.12.1	Per JCB-07-059 • Added Figure 3 – x16 NOR/NAND Flash + PSRAM + SRAM Shared Bus • Renumbered subsequent figures
3.12.1	Per JCB-07-048 Added Figure 8 – x16/x32 LPDRAM (SDR/DDR) and x8 eMMC Flash in 0.50mm ball pitch LFBGA
3.12.2	Per JCB-07-046 Resequenced the figures to keep like with like. Added Figure 7 – Ball Outline - Option BA: (x16 AD Mux NOR/x16 NAND) + (x16 DDR LPSDRAM) split bus, 128-Ball BGA, 0.65 mm Pitch, 12 mm x 12 mm Package Added Figure 8 – Ball Outline - Option BB: (x16 NAND) + (x16 DDR NOR/LPSDRAM) split bus 128-Ball BGA, 0.65 mm Pitch, 12 mm x 12 mm Package
4.1.2.10	Per JCB-07-085 Updated Section, Annex J: Serial Presence Detect (SPD) for DDR2 SDRAM, to Revision 1.3
4.1.2.10	Editorial Added Revisions 1.0 and 1.2 of the SPD back into 21C, so that all three Rev levels are represented in the Standard.
4.1.3	Per JCB-07-047 Added Section, Definition of the EE1002 and EE1002A Serial Presence Detect (SPD) EEPROMS
4.20	Updated Table of Contents
4.20.11	Per JCB-07-086 Updated Section, PC2-6400/PC2-5300/PC2-4200/PC2-3200 DDR2 SDRAM Unbuffered SO-DIMM Reference Design Specification, Rev. 2.4
4.20.17	Per JCB-07-002 Added Section, PC3-12800 DDR3 Unbuffered MicroDIMM Design Specification, Revision 0.34
4.20.18	Per JCB-07-057 Added Section, PC3/6400/OC3-8500/PC3-10600/PC3-12800 DDR3 Unbuffered SO-DIMM Design Specification, Revision 0.55
6	Added References to: • JESD208, Specialty DDR2-1066 SDRAM • JESD209, Low Power Double Data Rate (LPDDR) SDRAM Standard •
A-1	Updated Annex A (Informative) Differences between Release 17 and Release 16 of JESD21C.

Annex A.2 (informative) Differences between JESD21C, Release 16, and JESD21C, Release 15.

This table briefly describes most of the changes made to this standard, JESD21C, Release 16, compared to its predecessor, JESD21C, Release 15. Some editorial changes are not included.

Section/ Page	Description of Change
3.5.2-5	Updated Table of Contents
3.5.2-31, 32	Per JCB-06-038 Added Figure 20 – 16Mb to 512 Mb (x16) Synchronous 1.8V / 3.0V FEEPROM IN 56-PIN TSOP I
3.5.2-33, 34	Per JCB-06-038 Added Figure 21 – 16 Mb to 1Gb (x16) Synchronous 1.8V / 3.0V FEEPROM IN 64-BALL LFBGA I
3.7.7-3, 4	Updated Table of Contents
3.7.7-20	Per JCB-05-147 Rescinded Figure 14 – X16/18 BURST SRAM WITH COMMON I/O IN 221 BGA
3.7.7-22	Per JCB-05-147 Rescinded Figure 16 – X16/18 SIGMA SRAM WITH COMMON I/O IN 221 BGA
3.7.7-24	Per JCB-05-147 Rescinded Figure 18 – X18 SIGMA SRAM WITH SEPARATE I/O IN 221 BGA
3.7.8-2, 3, 4	Updated Table of Contents
3.7.8-11	Per JCB-05-147 Rescinded Figure 7 – 16K TO 256K BY 36 & 72 BURST SRAM IN BGA
3.7.8-12	Per JCB-05-147 Rescinded Figure 8 – X32/36 BURST SRAM WITH COMMON I/O IN 221 BGA
3.7.8-14	Per JCB-05-147 Rescinded Figure 10 – X32/36 SIGMA SRAM WITH COMMON I/O IN 221 BGA
3.7.8-16	Per JCB-05-147 Rescinded Figure 12 – X36 SIGMA SRAM WITH SEPARATE I/O IN 221 BGA
3.7.9-2	Updated Table of Contents
3.7.9-3	Per JCB-05-148 Updated Figure 1 – X64/X72 Burst SRAM with Common I/O in 209 BGA
3.7.9-4	Per JCB-05-147 Rescinded Figure 2 – X64/72 BURST SRAM WITH COMMON I/O IN 221 BGA
3.7.9-6	Per JCB-05-147 Rescinded Figure 4 – X64/72 SIGMA SRAM WITH COMMON I/O IN 221 BGA
3.8-3	Updated Table of Contents
3.8-11, 12	Per JCB-06-065 Added Figure 7 – 16Mb though 512Mb PSRAM in 6x8mm and 8x10mm 54-ball VFBGA
3.11.5.8	Added Section, GDDR4 Specific SGRAM Functions, incorporating the following BoD ballots: JCB-06-007, JCB-06-008, JCB-06-011, JCB-06-013, JCB -06-014, JCB-06-015

Annex A.2 (informative) Differences between JESD21C, Release 16, and JESD21C, Release 15.

This table briefly describes most of the changes made to this standard, JESD21C, Release 16, compared to its predecessor, JESD21C, Release 15. Some editorial changes are not included.

Section/ Page	Description of Change
3.12	Added Section, Multi-Chip Packages (MCP), incorporating the following BoD ballots: JCB-04-065, JCB-05-062, JCB-05-135, JCB-06004, JCB-06-009, JCB-06-010, JCB-06-028, JCB-06-040, JCB -06-061
4.1.2.7	Per JCB-06-016 Updated Section, Appendix X: Serial Presence Detect (SPD) for Fully Buffered DIMM, to Revision 1.1
4.20	Updated Table of Contents
4.20.7	Per JCB-06-044 Updated Section. PC2700/PC3200 SDRAM Registered DIMM, to Revision 2.2
4.20.10	Per JCB-06-043 Updated Section, PC2-6400/PC2-5300/PC2-4200/PC2-3200 Registered DIMM, to Revision 3.4
4.20.13	Per JCB-06-029 Updated Section, PC2-5300/PC2-6400 DDR2 SDRAM Unbuffered DIMM, to Revision 2.0
4.20.14	Per JCB-06-045 Added Section, PC2-4200/PC2-3200 DDR2 Registered Mini-DIMM, Revision 2.0
4.20.15	Per JCB-06-047 Added Section, PC2-4200/PC2-5300/PC2-6400 DDR2 Fully Buffered DIMM, Revision 3.0
4.20.16	Per JCB-06-064 Added Section, EP2-2100 DDR2 SDRAM 32b-SO-DIMM, Revision 1.0
6	Added References to JESD79-2 and JESD79-3
A-1	Updated Annex A (Informative) Differences between Release 16 and Release 15 of JESD21C.

A.3 (informative) Differences between JESD21C, Release 15, and JESD21C, Release 14.

This table briefly describes most of the changes made to this standard, JESD21C, Release 15, compared to its predecessor, JESD21C, Release 14. Some editorial changes are not included.

Section/ Page	Description of Change
3.7.7-4	Updated Table of Contents
3.7.7-14	Per JCB-05-093 Updated Figure 8 – 64K to 64M by 16 & 18 SDRAM and SSRAM in TQFP
3.7.7-15	Per JCB-05-097 Updated Figure 9 – 64K to 64M by 16 & 18 Burst SSRAM in BGA
3.7.7-16	Per JCB-05-094 Updated Figure 10 – 256K to 64M by 16 & 18 Network SSRAM in 119 BGA
3.7.7-18	Per JCB-05-096 Updated Figure 12 – 64K to 16M by 16 & 18 Burst SSRAM in TQFP
3.7.7-21	Per JCB-05-092 Updated Figure 15 – x16/18 Network/SIGMA SRAM with Common I/O in 209 BGA
3.7.7-26	Per JCB-05-098 Updated Figure 20 – 1Gb Density in x16/18 Burst SRAM with Common I/O in 165 BGA
3.7.7-27	Per JCB-05-095 Updated Figure 21 – 1Gb Density in x16/18 Network SRAM with Common I/O in 165 BGA
3.7.8-2, 3, 4	Updated Table of Contents
3.7.8-5	Per JCB-05-096 Updated Figure 1 – 32K to 8M by 32 & 36 Burst SSRAM in TQFP
3.7.8-6	Per JCB-05-093 Updated Figure 2 – 32K to 32M by 32 & 36 SDRAM and SSRAM in TQFP
3.7.8-7	Per JCB-05-097 Updated Figure 3 – 32K to 32M by 32 & 36 Burst SSRAM in BGA
3.7.8-8	Per JCB-05-094 Updated Figure 4 – 128K to 32M by 32 & 36 Network SSRAM in 119 BGA
3.7.8-19	Per JCB-05-098 Updated Figure 15 – 1Gb Density in x32/36 Burst SRAM with Common I/O in 165 BGA
3.7.8-20	Per JCB-05-095 Updated Figure 16 – 1Gb Density in x32/36 Network SRAM with Common I/O in 165 BGA
3.8-3	Updated Table of Contents
3.8-6	Per JCB-05-133 Added Figure 6 – 8M to 64M by 16 Burst PSRAM in FBGA
3.11.4-7	Updated Table of Contents
3.11.4-43	Per JCB-04-003A Added Figure 36 – 8M, 16M, & 32M x 32 Low Power DDR SDRAM in 90-Ball FBGA

A.3 (informative) Differences between JESD21C, Release 15, and JESD21C, Release 14.

This table briefly describes most of the changes made to this standard, JESD21C, Release 15, compared to its predecessor, JESD21C, Release 14. Some editorial changes are not included.

Section/ Page	Description of Change
3.11.5.7-7	Per JCB-05-040 Added GDDR3 SGRAM Read Timing
3.11.5.7-14	Per JCB-05-016 Added GDDR3 SGRAM Boundary Scan
3.11.5.7-18	Per JCB-05-017 Added GDDR3 SGRAM tFAW Definition
3.11.5.7-19	Per JCB-05-036 Added GDDR3 SGRAM Mode Register
4.20-1	Updated Table of Contents
4.20.7-1	Per JCB-05-136 Updated Section to Revision 2.09
4.20.10-1	Per JCB-05-106 Updated Section to Revision 3.2
4.20.13-1	Per JCB-04-082 Updated Section to Revision 1.1
A-1	Updated Annex A (Informative) Differences between Release 15 and Release 14 of JESD21C.

A.4 Differences between JESD21C, Release 14, and JESD21C, Release 13.

This table briefly describes most of the changes made to this standard, JESD21C, Release 14, compared to its predecessor, JESD21C, Release 13. Some punctuation changes are not included.

Section/ Page	Description of Change
3.5.1-4	Updated Table of Contents
3.5.1-37	Per JCB-03-084 Added new Figure 23 – 2-Wire EEPROM, MLP 2x3 MM Pinout
3.5.2-4	Updated Table of Contents
3.5.2-26	Per JCB-03-036 Added new Figure 17 – 128Mb to 1Gb (x8/x16) FEEPROM in 64-Ball LBGA
3.5.2-27	Per JCB-03-037 Added new Figure 18 – 128Mb to 1Gb (x8/x16) FEEPROM in 64-Ball TFBGA
3.5.2-28	Per JCB-04-083 Added new Figure 19 – 16Mb to 256Mb (x8/x16) FEEPROM in 56-Pin TSOP II
3.5.3-2	Updated Table of Contents
3.5.3-19	Per JCB-04-018 Added new Section, 3.5.3.6, EEPROM with Two SPD Software Write Protect Methods.
3.7.7-4	Updated Table of Contents
3.7.7-28	Per JCB-04-043 Added new Figure 22 – 52-Pin TSOP II Pin Assignment for Low Power SRAMs
3.11.4-7	Updated Table of Contents
3.11.4-42	Per JCB-04-003A Added new Figure 35 – 8M x 15 DDR SDRAM in 78-Ball TFBGA
3.11.4-43	Per JCB-04-072 Added new Figure 36 – 8M, 16M, & 32M X32 Low Power DDR SDRAM in 90-Ball FBGA
3.11.5.7-1	Added new Section 3.11.5.7, GDDR3 Specific SDRAM Functions, incorporating the following ballots: JCB-04-025 JCB-04-026 JCB-04-027 JCB-04-032 JCB-04-033 JCB-04-034 JCB-04-059 JCB-04-067
4.1-1	Updated Table of Contents
4.1.2.10	Per JCB-04-005 and JCB-04-099 Updated Section to Revision 1.2
4.20-1	Updated Table of Contents
4.20.7-1	Per JCB-04-001 Updated Section to Revision 2.0.

A.4 Differences between JESD21C, Release 14, and JESD21C, Release 13.

This table briefly describes most of the changes made to this standard, JESD21C, Release 14, compared to its predecessor, JESD21C, Release 13. Some punctuation changes are not included.

Section/ Page	Description of Change
4.20.9-1	Per JCB-04-053 Updated Section to Revision 1.1.
4.20.10-1	Per JCB-04-049 Added new Section, 4.20.10. 240-Pin PC2-3200/PC2-4300 DDR2 SDRAM Registered DIMM Reference Design Specification, Rev. 1.0
4.20.11-1	Per JCB-04-052 Added new Section, 4.20.11. 200-Pin PC2-4200/PC2-3200 DDR2 SDRAM Unbuffered SO-DIMM Reference Design Specification, Rev. 0.52
4.20.12-1	Per JCB-04-054 Added new Section, 4.20.12. 200-Pin PC2-4200/PC2-3200 DDR2 SDRAM Unbuffered MicroDIMM Reference Design Specification, Rev. 0.5
4.20.13-1	Per JCB-04-082 Added new Section, 4.20.13. 240-Pin PC2-3200/PC2-4300 DDR2 SDRAM Unbuffered DIMM Reference Design Specification, Rev. 1.0
A-1	Updated Annex A (Informative) Differences between Release 14 and Release 13 of JESD21C.

A.5 Differences between JESD21C, Release 13, and JESD21C, Release 12.

This table briefly describes most of the changes made to this standard, JESD21C, Release 13, compared to its predecessor, JESD21C, Release 12. Some punctuation changes are not included.

Section/ Page	Description of Change
3.10.3-2	Updated Table of Contents
3.10.3-12	Per JCB-03-078 Added new Figure 10 – 8M x 32 GDDR3 Graphics RAM in 144-Ball FBGA
3.11.2-4	Updated Table of Contents
3.11.2-23	Editorial correction to the caption, ball-out label, and addressing scheme placeholders of Figure 19.
3.11.2-25	Per JCB-03-002 Added new Figure 21 – 64M, 128M, 256M, 512M, & 1G by 4 by 2 DDR2 SDRAM in Stacked FBGA
3.11.2-26	Per JCB-03-024 Added new Figure 22 – 64M, 128M, 256M, 512M, & 1G by 4 by 2 DDR2 SDRAM for Stacked FBGA Requiring Support Balls
3.11.3-4	Updated Table of Contents
3.11.3-25	Editorial correction to the caption, ball-out label, and addressing scheme placeholders of Figure 21.
3.11.3-27	Per JCB-03-002 Added new Figure 23 – 32M, 64M, 128M, 256M, & 512M by 8 by 2 DDR2 SDRAM in Stacked FBGA
3.11.3-28	Per JCB-03-024 Added new Figure 24 – 32M, 64M, 128M, 256M, & 512M by 8 by 2 DDR2 SDRAM for Stacked FBGA Requiring Support Balls
3.11.4-7	Updated Table of Contents
3.11.4-35	Per JCB-03-047 and JCB-03-057 For Figure 28 – 2M, 4M, & 8M by 32 SDR Low Power SDRAM in 90-Ball LFBGA • Changed ball H3 from “NC” to “NC,A12” • Changed ball H7 from “NC,A12” to “NC” • Change ball M1 from “VSS” to “VSSQ” • Added a column for 512Mb (16M x 32) to the Addressing Scheme table. • Added 16M to the Figure caption and ball-out label.
3.11.4-37	Editorial correction to the caption, ball-out label, and addressing scheme placeholders of Figure 30.
3.11.4-39	Per JCB-03-025 Added new Figure 32 – 16M, 32M, 64M, 128M, & 256M by 16 by 2 DDR2 SDRAM in Stacked FBGA
3.11.4-40	Per JCB-03-024 Added new Figure 33 – 16M, 32M, 64M, 128M, & 256M by 16 by 2 DDR2 SDRAM for Stacked FBGA Requiring Support Balls
3.11.4-41	Per JCB-03-055 Added new Figure 34 – 4M x 32 DDR2 SDRAM in 144-Ball FBGA
3.11.5-2	Updated Table of Contents
3.11.5.2-16	Per JCB-03-050 Added new Section 3.11.5.2.13 – MRS/EMRS for Low Power DDR SDRAM

A.5 Differences between JESD21C, Release 13, and JESD21C, Release 12.

This table briefly describes most of the changes made to this standard, JESD21C, Release 13, compared to its predecessor, JESD21C, Release 12. Some punctuation changes are not included.

Section/ Page	Description of Change
3.11.5.5-1	Per JCB-03-045 Added new Section 3.11.5.5 – DDR2 Specific SDRAM Functions
3.11.5.6-1	Per JCB-03-051 and JCB-03-052 Added new Section 3.11.5.6 – GDDR2 Specific SDRAM Functions
4.1-1	Updated Table of Contents
4.1.2.4-1	Per JCB-03-059 Updated Section 4.1.2.4 – Appendix D : Specific SPDs for DDR SDRAM to Revision 1.0. Entire section replaced with the ballot material.
4.1.2.10	Per JCB-03-011 Added new Section 4.1.2.10 – Appendix X : Specific SPDs for DDR SDRAM, Revision 1.0
4.20-1	Updated Table of Contents
4.20.6-1	Per JCB-03-010 Added PC3200 to the PC2700 UnBuffered SO-DIMM Specification. Entire section replaced with the ballot material.
4.20.8-1	Per JCB-03-009 Added PC3200 to the PC2700 UnBuffered TSOP DIMM Specification. Entire section replaced with the ballot material.
4.20.9-1	Per JCB-03-004 Added new Section 4.20.9 – 100-Pin DDR SDRAM Unbuffered 32b DIMM Reference Design Specification. .
A-1	Added Annex A (Informative) Differences between Release 13 and Release 12 of JESD21C.